CLAIMS

1. An integrated circuit device adapted to be incorporated into a portable article having a memory, the device comprising at least:

a central processor unit;

at least one memory;

at least one data input/output pad;

n address bus lines connecting the central processor unit to the memory and/or to the input/output pad to carry address bits; and

p data bus lines connecting the central processor unit to the memory and/or to the input/output pad for conveying data bits;

wherein at least one line from the address bus lines and the data bus lines is associated with an additional line for conveying bits that are complementary to the bits conveyed over said at least one line.

2. A device according to claim 1, wherein the additional line has a capacitance equivalent to a capacitance of the address bus line or the data bus line with which it is associated.

3. A device according to claim 1, wherein each of the n address bus lines is associated with a respective additional line.

4. A device according to claim 1, wherein each of the p data bus lines is associated with a respective additional bus line.

5. A device according to claim 3, wherein the complementary bits on the additional lines form data or address logic values that are complementary to the logic values conveyed by the bus.

6. A device according to claim 1, wherein for each line, a dual amplifier is used.